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EXPEDITED PROCEDURE - EXAMINING GROUP 2187

November 6, 2002

Official


Time: 1:35 pm
 (Minneapolis, Minn.)

TO: Commissioner for Patents
 Attn: Than Vinh Nguyen
 Patent Examining Corps
 Facsimile Center
 Washington, D.C. 20231

FROM: Viet V. Tong

OUR REF: 303.663US1

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* Please deliver to Examiner Than Vinh Nguyen in Art Unit 2187. *

Document(s) Transmitted: Amendment & Response under 37 CFR § 1.116 (5 pgs); Clean Version of Pending Claims (7 pgs.).

Total pages of this transmission, including cover letter: 13 pgs
 If you do NOT receive all of the pages described above, please telephone us at 612-373-6900, or fax us at 612-339-3061.

In re. Patent Application of: Eugene H. Cloud

Examiner: Than Vinh Nguyen

Serial No.: 09/518,338

Group Art Unit: 2187

Filed: March 3, 2000

Docket No.: 303.663US1

Title: HIGH DENSITY STORAGE SCHEME FOR SEMICONDUCTOR MEMORY

Please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

By: 
 Name: Viet V. Tong
 Reg. No.: Reg. No. 45,416

I hereby certify that this paper is being transmitted by facsimile to the U.S. Patent and Trademark Office on the date shown below.

Amy J. Moriarty
 Amy J. Moriarty

November 6, 2002
 Date of Transmission

EXPEDITED PROCEDURE - EXAMINING GROUP 2187

Patent
11/13/02
JRWS/N 09/518,338IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Eugene H. Cloud

Examiner: Than Vinh Nguyen

Serial No.: 09/518,338 ✓

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Title: HIGH DENSITY STORAGE SCHEME FOR SEMICONDUCTOR MEMORYAMENDMENT & RESPONSE UNDER 37 C.F.R. § 1.116

Box AF
 Commissioner for Patents
 Washington, D.C. 20231

In response to the Final Office Action mailed August 22, 2002, please amend the application as follows:

IN THE CLAIMS

Please substitute the claim set in the appendix entitled Clean Version of Pending Claims for the previously pending claim set. The substitute claim set is intended to reflect amendment of previously pending claims 6-9, 11, 15, and 18-21. The specific amendments to individual claims are detailed in the following marked up set of claims.

6. (Amended) A memory device comprising:

an input/output buffer;
 a cache memory connected to the input/output buffer;
 a compression and decompression engine connected to the cache memory; and
 a volatile main memory connected to the compression and decompression engine,
 wherein the input/output buffer, the cache memory, the compression and decompression engine,
 and the volatile main memory are located in a single chip.

7. (Amended) The memory device of claim 6 wherein the compression and decompression engine is connected between the volatile main memory and the cache memory.